ABSTRACT OF THE DISCLOSURE

A data amplifier configured to allow for fewer data lines and/or increased processing speeds. Specifically, multiple helper flip-flops are used to prefetch data in a data amplifier. The helper flip-flops are configured to latch one or two of the data bits from a 4-bit prefetch in an alternating periodic fashion, thereby necessitating fewer data lines. Alternatively, the number of data lines can be maintained and faster bus processing speeds may be realized.